REMARKS

Applicant requests that the previously filed and unentered amendments not be entered.

The comments of the applicant below are each preceded by related comments of the examiner (in small, bold type).

The comments below are in response to the office communication of November 26, 2004.

> **Continuation of 2. NOTE: The amendment made to the independent claims do not reduce the scope of the claim limitations nor do they change the limitations presently found in the claims.**
>
> **Continuation of 5. does NOT place the application in condition for allowance because: Applicant argues in essence on page 7 "This clearly describes a situation where the future file cannot e restored in a single clock cycle". This has not been found persuasive. The future file and current file of the invention are embodied in Kishigami's register file 203 in Figure 10B and explained in column 14, lines 25-61. Kishigami teaches in column 15, line 58 to column 16, line 16 that swapping the registers, i.e. restoring the data in the future file takes one cycle (Kishigami column 16, lines 7-10). Kishigami's device embodies not only the improved aspects, i.e. restoring the register data in one cycle, but also features from the pototype, i.e. restoring the register data in 16 cycles.**

The claims have been further amended. Even if Kishigami does disclose restoring the registers that it uses in place of a future file in one clock cycle, its reference to a future file that is restored in more than once clock cycle (col. 18, ll. 18-19) makes clear that *that* future file cannot be restored in more than one clock cycle. Kishigami does not disclose a processor that is "capable of restoring its future file in a single clock cycle," and that nonetheless restores it in more than one clock cycle.

The comments below are in response to the office action of August 12, 2004.

> **7. Claim 6 recites the limitation "the number of clock cycles it takes to flush a pipelined processor" on its second and third lines. It is unclear whether this "number of clock cycles" can be determined from any arbitrary pipelined processor, a pipelined processor that is associated with the future file of claim 1, or something else altogether. Please clarify the claim language to more clearly define the metes and bounds of the claimed invention.**

Claim 6 has been amended.

9. Claims 1-3, 6-8, 12, 15 and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Kishigamietal., U.S. Patent No. 5,155,817.

10. Regarding claim 1, Kishigami has taught a method comprising

a. Accessing a future file which is capable of being restored in a single clock cycle (see Col. 8 lines 28-35 and Col. 15 line 47 — Col. 16 line 12).
b. Restoring a future file over more than one clock cycle when a termination occurs (see Col 18, lines 16-19, 42-45).

Claim 1 has been amended to recite a processor which is capable of "restoring [its] future file in a single clock cycle" but which "restor[es] the future file over more than one clock cycle." Kishigami does not teach or suggest the existence of a processor which restores its future file over more than one cycle when it could restore the same future file in a single clock cycle.

The first passage of Kishigami cited by the examiner describes a future file that is updated in normal operation "immediately" after the execution of instructions, but does not describe or suggest (in the words of claim 1) "restoring the future file" (col. 8 lines 28-35). The second passage cited describes a solution that replaces the future file and current file with a common set of registers, which may allow a process comparable to restoration to be performed in a single clock cycle, but it does not describe or suggest performing this restoration step over more than one clock cycle (col. 15 line 47 – col. 16 line 12). The third passage cited does indicate that restoration is done over more than one cycle, but it notes that this is because "at least 16 cycles are needed if there are 16 general purpose registers," (emphasis added) (col. 18 lines 18-19). This clearly describes a situation where the future file *cannot* be restored in a single clock cycle.

13. Regarding claims 7 and 15, taking claim 15 as exemplary, Kishigami has taught a system comprising:

a. A static random access memory device (204 of Fig.9),

b. A processor coupled to the static random access memory device, wherein the processor includes a first set or registers, a second set of registers, a pipeline and a control unit (see Col.8 lines 22-34 and Fig. 1) capable of restoring the first registers with data contained in the second registers during a single clock cycle (see Col. 8 lines 28-35 and Col. 15 line 47 — Col. 16 line 12), but adapted to restore at least some of the registers in the first set of registers with values in at least some of the registers in the second set of registers over more than one clock cycle if a

termination occurs in the pipeline (see Col. 4 lines 42-46 and Col. 18 lines 16- 19, *42-45).*

14. Claim 7 is nearly identical to claim 15. Claim 7 differs in its lack of a static random access memory device and a processor coupled to said memory device, but encompasses the same scope as claim 15 Therefore, claim 7 is rejected for the same reasons as claim 15.

Claims 7 and 15 have been amended and are patentable for at least the same reasons as claim 1.

40. On p 10 lines 11-15 of the present amendment, the Applicant argues, in essence:

"Therefore, it is clear that the only time that Kishigami will restore the future file over more than one clock cycle, is when that is the only alternative. More specifically, whenever the future file is capable of being restored over a single clock cycle, it will be so restored."

41. The Examiner would like to point out that the Applicant is admitting that the prior art of reference, namely Kishigami, has taught all of the limitations of amended claims 1,7 and 15, specifically that Kishigami has taught a future file capable of being restored over a single clock cycle, and the restoring of the future file over more than one clock cycle when a termination occurs.

The applicant wishes to clarify its prior argument with respect to Kishigami. The applicant believes that the only example of restoring a future file in Kishigami describes restoring the future file over 16 clock cycles and states that this is "needed [because] there are 16 general purpose registers" in the prototype of that example. There is no example in Kishigami of restoring a future file over one cycle. Kishigami identifies the requirement of multiple clock cycles as a problem, but solves it by eliminating the future file, not by describing a way to restore it in one clock cycle. The combined future file and current file in Kishigami may execute in one cycle a task comparable to restoring the future file. In any event, Kishigami neither discloses nor suggests a processor which "is capable of restoring [its] future file in a single clock cycle" but which in fact "restor[es] the future file over more than one clock cycle." The applicant recants any statement previously made that is inconsistent with what is said in this paragraph.

42. On p.11 lines 1-13 of the present amendment, the Applicant argues, in essence:

"Kishigami does not teach or suggest a future file "which is capable of being restored in a single clock cycle" but yet is restored "over more than one clock cycle when the termination occurs" as defined in claim 1. Rather, Kishigami teaches that a special prototype which requires multiple clock cycles to restore the future file is restored over

those multiple clock cycles, but only because that is absolutely necessary. Kishigami describes the general undesirability of restoring a future file over multiple clock cycles. This demonstrates the unobviousness of the present system which specifically teaches restoring a future file over more than one clock cycle even though that future file is capable of being restored in a single clock cycle."

43. However, Kishigami has taught a future file which is capable of being restored in a single clock cycle but is restored over more than one clock cycle when a termination occurs (see above paragraphs 10, 13 and 14). In fact, the Applicant has admitted that Kishigami has taught such a future file (see p.10 lines 11-15 of the present amendment filed on 5/06/2004).

The applicant respectfully disagrees for the reasons set forth in response to the Examiner's comment 41.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended a claim does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

Please apply any charges or credits to deposit account 06-1050, reference 10559-393001.

Respectfully submitted,

Date: 12/27/4

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